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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,647	07/29/2003	Jeffery Steven Beck	10030328-1 (2116-21-3)	8261

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EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,647	BECK ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/29/2003 & 7/6/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/29/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. **Figure 3** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2, 17 & 18 are objected to because of the following informalities:

Claim 2 recites "**the** row trace" in the second line of the claim, which should be corrected to read as -- a row trace --.

Claim 17 recites "**the** level at a second control node" which should be also corrected to read as -- a level at a second control node --.

Claim 18 recites "**the** level at a third node" which should be corrected to read as -- a level at a third node --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8 recites the limitation "the pixel-capture structure" and "the structure". There is insufficient antecedent basis for these limitations in the claim. Although the independent claim 1 recites "A pixel-capture circuit, comprising:...", there is no limitation "structure."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5, 6, 9, 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroda et al. (US 6,512,543 B1).

Regarding claim 1, Kuroda discloses a pixel-capture circuit (Fig. 3), comprising:

a pixel-capture device (photodiode 33 shown in Fig. 3) having a node (a node at the positive electrode of the photodiode 33) and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel (see col. 6, lines 53-56);

a row node (a node at line 41 connected to the gate of row select transistor 42) carrying a row signal (i.e., Vdd on line 41) that is operable to couple the node to a column trace (43) during a read of the captured pixel and operable to set the node to a predetermined signal level (reset to Vdd level by transistor 60) during a reset phase (see Fig. 3 and col. 8, line 52 – col. 9, line 5 and note the timing diagram in Fig. 2).

Regarding claim 2, Kuroda also discloses a reset trace (49) carrying a reset signal (ΦR by control signal from line 37 shown in Fig. 3) that is operable to uncouple the node from the row trace during the reading of the captured pixel (see Fig. 2 and col. 7, line 36 – col. 8, line 40).

Regarding claim 3, as clearly disclosed in col. 6, lines 13-14 that the pixel-capture unit device is disposed on a silicon substrate (inherent substrate by virtue of solid-state image sensor).

Regarding claim 5, Kuroda clearly discloses a photodiode (33) in Fig. 3.

Regarding claim 6, further discloses by Kuroda is that the pixel signal is a voltage (electrical potential) as described in col. 6, lines 53-57.

Regarding claim 9, a pixel-capture circuit (Fig. 3), comprising:

a pixel-capture device (photodiode 33) having a first and second node, the first node coupled to a first supply node (ground);

a first transistor (35) having a control node (a gate node), a first drive node (a source node connected to line 41), and a second drive node (a drain node connected to transistor 42), the control node coupled to the second node of the pixel-capture device and the first drive node coupled to a second supply node (power supply Vdd via line 41);

a second transistor (42) having a control node (a gate node connected to line 41), a first drive node (the node connected to the drain of transistor 35), and a second drive node (a node connected to the column readout line 43), the control node of the second transistor coupled to a row node (the node on line 41), the first drive node of the second transistor (42) coupled to the second drive node of the first transistor (35), the

second drive node of the second transistor coupled to a column node (see Fig. 3 and col. 8, line 51 – col. 9, line 5);

a third transistor (60) having a control node (a gate node), a first drive node (a node connected to photodiode 33), and a second drive node (a node connected to line 41), the control node of the third transistor coupled to a reset node (the common node of the photodiode 33, transistor 35 and transistor 60), the first drive node of the third transistor coupled to the row node (a node on line 41), the second drive node of the third transistor coupled to the second node of the of the pixel-capture device (see Fig. 3 and col. 8, line 51 – col. 9, line 5).

Regarding claim 16, Kuroda discloses a method, comprising:

integrating an amount of light (by photodiode 33 shown in Fig. 3);

generating a signal on a pixel node (the node connected to the gate of transistor 35), the signal having a level related to the integrated amount of light (see Fig. 3; col. 6, lines 53-57); reading the signal in response to a first control signal (a control signal on line 37 that releases Vdd through transistor 40) on a first control node (a common node at line 37 that connects all nodes on lines 41 to the gate of transistor 42); and resetting the signal level at the pixel node (resetting to Vdd on line 41 by reset transistor 60) in response to a second control signal (reset pulse ΦR) on the first control node (see Fig. 3 and col. 8, line 51 – col. col. 9, line 5 and note the timing chart shown in Fig. 2 for the operation).

Regarding claim 17, it is also clear in Figs. 2 & 3 of Kuroda that reading the signal comprises detecting a level at a second control node (the potential level amplified by transistor 35 the gate node of transistor 35 as described in col. 6, lines 53-57).

Regarding claim 18, Kuroda further discloses the resetting comprising: setting a level at a third control node (the gate node of reset transistor 60) to a predetermined high level (high level 76 of reset pulse ΦR as shown in Fig. 2); and pulsing the level of the first control node to a predetermined low level (row select pulse 66 is set to low level as shown in Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 7, 8, 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,512,543 B1) in view of Rhodes (US 6,812,539 B1).

Regarding claim 7, Kuroda discloses a substrate (an inherent substrate of the solid-state image sensor shown in Fig. 3) but Kuroda does not explicitly disclose two conductive layers disposed on the substrate; and one or more conductive paths

respectively operable to carry the row signal, each of the conductive paths disposed in a respective one of the two conductive layers.

However, Rhodes teaches an improvement in a pixel circuit layout for saving interconnection layers by routing conductive paths that carry row signals (e.g., path 36 of row select transistor and path 28 of reset transistor shown in Figs. 1 & 13) on two interconnection layers (a layer 44 and a layer containing transistor paths 36, 32, 28, etc. underneath of layer 44) on the silicon substrate as shown in Figs. 1 & 13 and col. 1, lines 56-67 and col. 4, lines 15-50).

Therefore, it would have been obvious to one of ordinary skill in the art at to layout the pixel-capture circuit of Kuroda by conductive paths respectively operable to carry the row signal, each of the conductive paths disposed in a respective one of the two conductive layers in view in view of the teaching of Rhodes so as to save conductive interconnection layers while mitigating undesired effects such as blooming, blurring, shadowing as suggested by Rhodes in col. 2, lines 15-21.

Regarding claim 11, Kuroda discloses all limitations of an imaging array as analyzed in claim 1 with additional disclosure of a plurality of pixel-capture circuits arranged in rows and columns (Fig. 3).

Kuroda is silent about the imaging array being a CMOS array. As taught by Rhodes, a CMOS image sensing array is disclosed, wherein the CMOS image sensing array can be implemented using 4T (4 transistors) or 3T (3 transistors) structure similar to the array structure of Kuroda (see Rhodes, Fig. 13 and col. 3, lines 26-44). It is also

well recognized in the art that the CMOS image sensing array provides advantages over conventional CCD array for its low power consumption, addressable pixel scheme and easy for manufacturing using very popular CMOS process.

Therefore, it would have been obvious to one of ordinary skill in the art at to combine the teachings of Kuroda and Rhodes to make a CMOS array to reduce power consumption of the array as well as reducing manufacturing cost by using the popular CMOS process.

Regarding claim 12, the limitations of this claim are also met by the analysis of claim 2 above.

Regarding claim 13, Kuroda in view of Rhodes also discloses a first conductive layer (layer 44) having the row trace and the reset trace (trace 50 that connects to reset transistor 28 and arranged in each row) disposed therein and a second conductive layer (the layer underneath layer 44) having the column trace (i.e., a trace connected to column node 38) disposed therein (see Figs. 1 & 13 and col. 4, lines 25-50).

Regarding claim 14, the combined teachings of Kuroda and Rhodes also discloses all limitations of claim 14 as analyzed in claim 11 above. Additionally, both Kuroda and Rhodes disclose a processor (a horizontal shift processing 52 shown in Fig. 3 of Kuroda or 260 shown in Fig. 12 of Rhodes) coupled with the CMOS array and

operable to facilitate a detection of a voltage signal at each column trace (signal on vertical transfer array) in each pixel in the CMOS array.

Regarding claim 15, both Kuroda and Rhodes disclose a memory (buffer 55 in Fig. 3 of Kuroda or RAM 310 in Fig. 14 of Rhodes) coupled to the processor and operable to store the pixel (see Kuroda, col. 7, lines 5-6 or Rhodes, col. 8, lines 44-50).

Regarding claim 10, since the combination of Kuroda and Rhodes teaches a CMOS image sensing array as analyzed in claim 11 above, the first, second and third transistors are MOSFET transistors by inherency.

Regarding claim 4, Kuroda discloses the pixel-capture unit circuit as analyzed in claim 1 but fails to explicitly disclose the row trace, the column trace, and the reset trace are disposed within no more than two conductive layers disposed on the silicon substrate.

However, Rhodes teaches an improvement in a pixel circuit layout for saving interconnection layers by routing row trace, column trace and reset trace on two interconnection layers (a layer 44 and a layer containing transistor paths 36, 32, 28, etc. underneath of layer 44) on the silicon substrate as shown in Figs. 1 & 13 and col. 1, lines 56-67 and col. 4, lines 15-50).

Therefore, it would have been obvious to one of ordinary skill in the art at to layout the pixel-capture circuit of Kuroda by disposing the row trace, the column trace

and the reset trace within no more than two conductive layers on the silicon substrate in view of the teaching of Rhodes so as to save conductive interconnection layers while mitigating undesired effects such as blooming, blurring, shadowing as suggested by Rhodes in col. 2, lines 15-21.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner